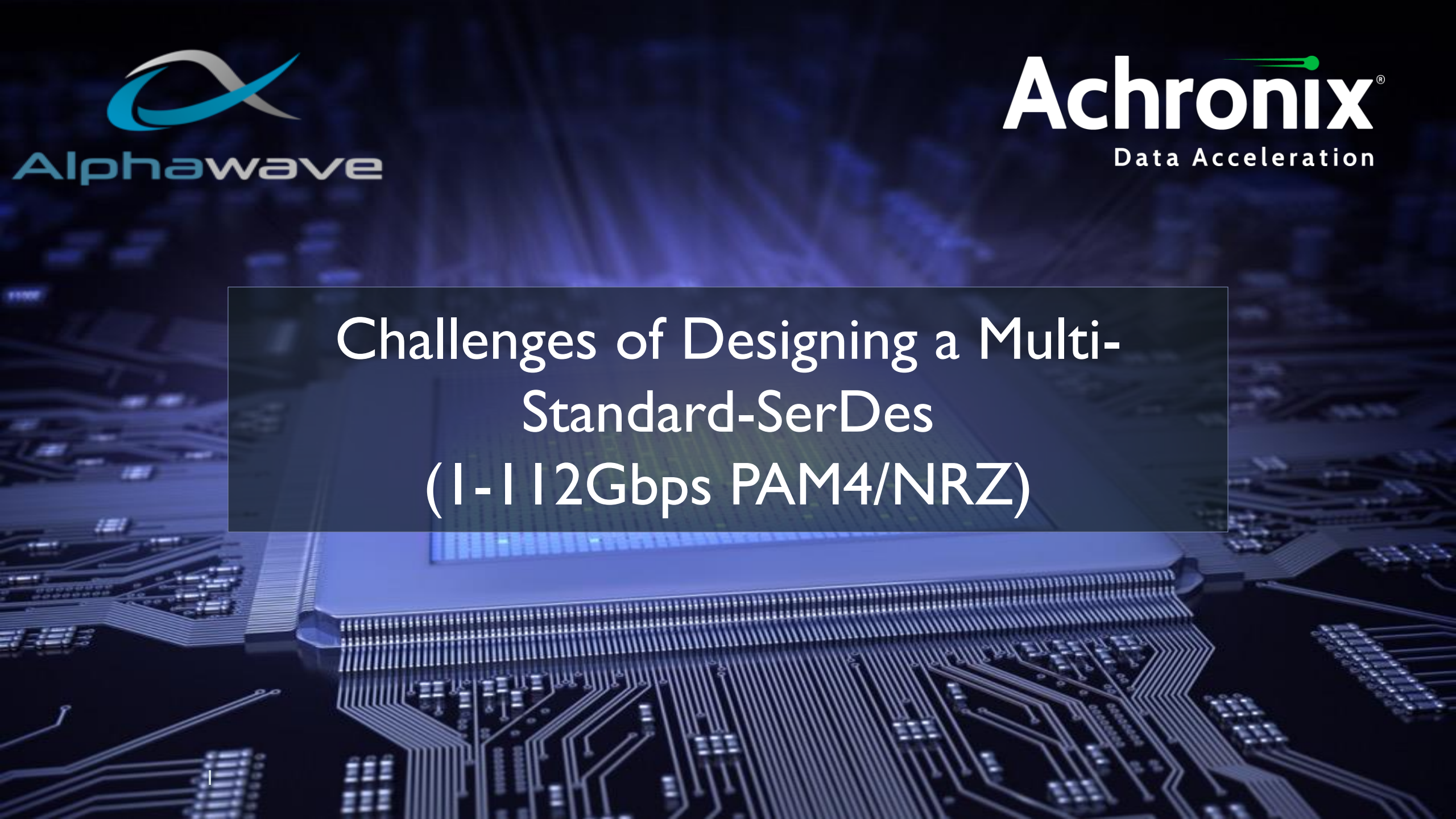
Alphawave
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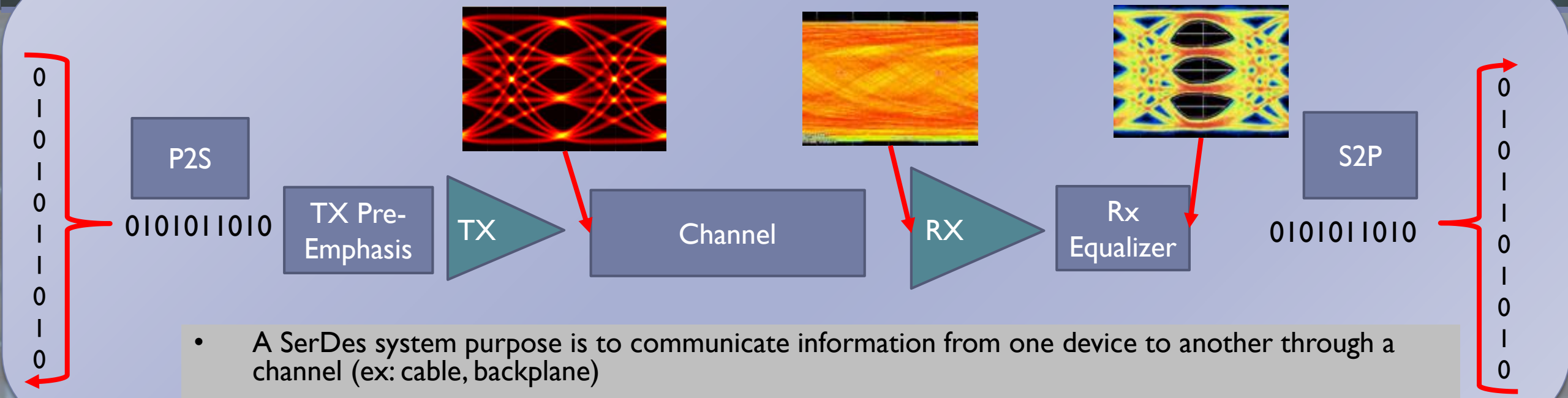
Data Acceleration
Challenges of Designing a Multi-Standard-SerDes (1-112Gbps PAM4/NRZ)

Challenges of Designing a Multi-Standard-SerDes 1-112Gbps PAM4/NRZ SerDes

Agenda

- SerDes Basics
- The Challenge
- Details on one of the many challenges
- Why make a Multi-Standard SerDes

SerDes System Basics



- A SerDes system purpose is to communicate information from one device to another through a channel (ex: cable, backplane)
- This starts with taking parallel data and serializing it before sending it through the channel. This allows for significantly less number of channels to be required to get information from point a to point b.
- The Channel degrades the signal due to signal integrity effects (ISI, Loss, Xtalk…)
- The Receiver (Rx) and it's equalizer then compensates for these effects and opens the eye back up.
- Then the data is parallelized through the serial to parallel (S2P) block

What makes a SerDes a Multi Standard SerDes

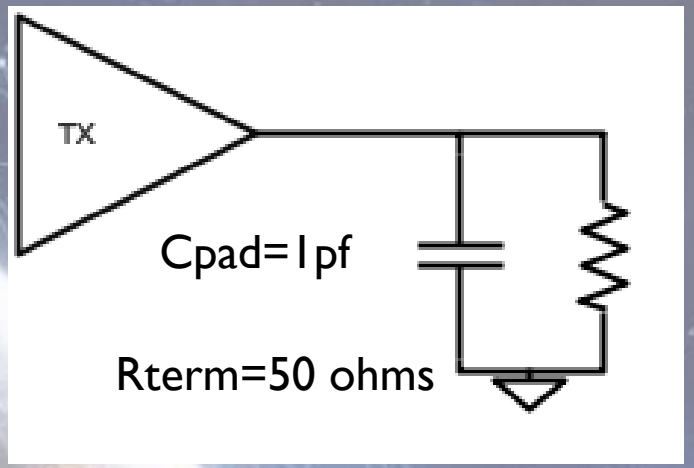
- Data Rate: 1-112Gbps SerDes with no holes
- Signaling: NRZ and PAM4
- Standards:
  - PCIE GEN1,2,3,4 and 5
  - Ethernet 10, 25, 40, 50, 100, 200 and 400 Gigabit Ethernet
  - CPRI
  - JESD204
  - Interlaken
  - OIF (XSR, VSR, MR, LR)

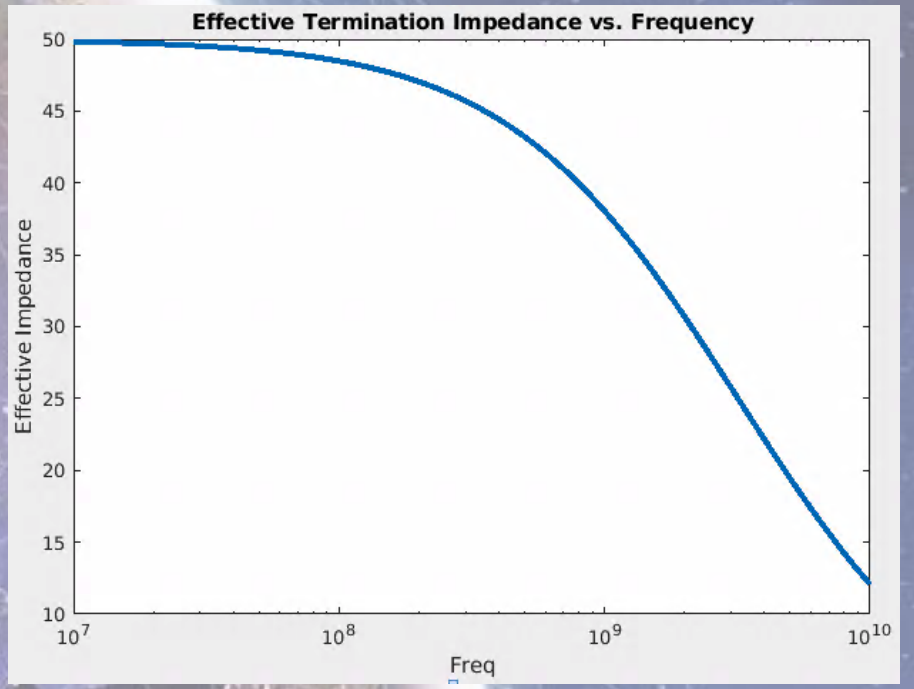
Challenges of Multi Standard Support for SerDes

- At design start focus is on top data rate 112Gbps
  - Optimizing clocking architecture
  - Optimizing equalization architecture
  - Optimizing digital interfaces
- There are many challenges supporting multiple standards. This Presentation will focus on one.
  - Legacy Rx/Tx detect requirements
- Key to success is early planning to accommodate these challenges

Challenge: Supporting legacy Rx detect requirements

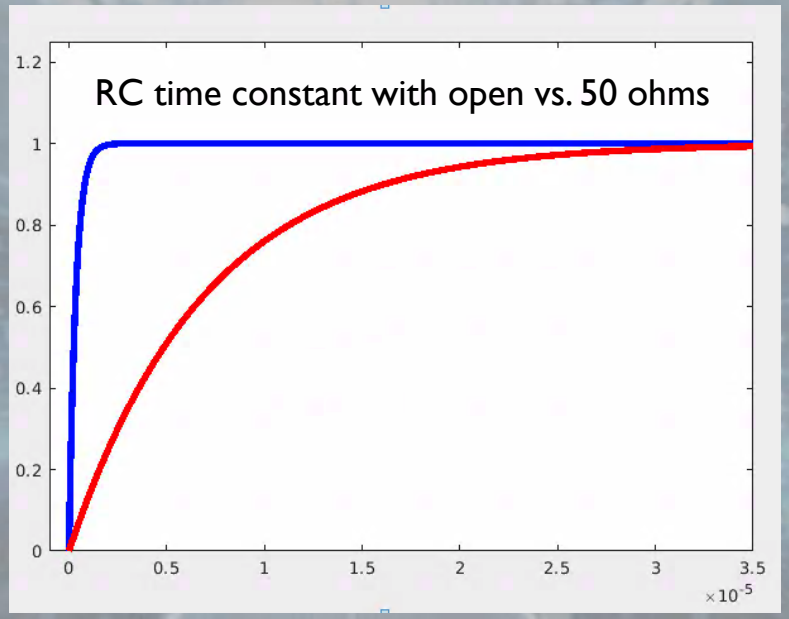
- Any loading on output of Tx or input of Rx changes the effective impedance vs. frequency of the termination
- Some standards have requirement for Tx to detect the presence of Rx
- This requires more loading on the output.
- For 112Gbps PAM4 operation the output of the Tx requires very high bandwidth and matched impedance



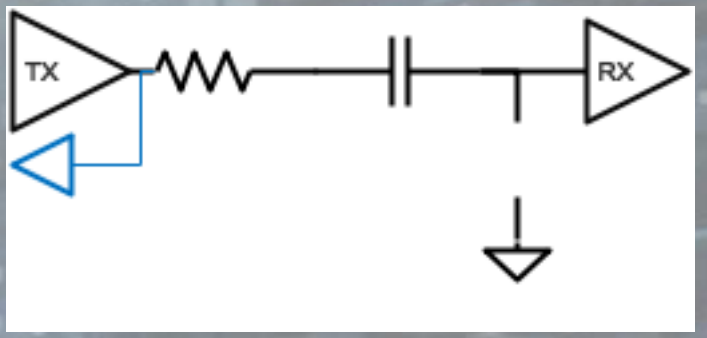


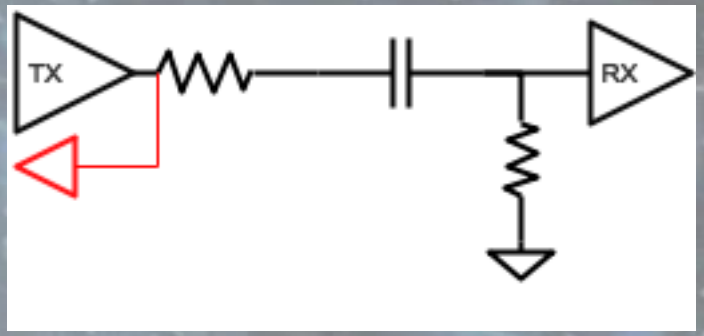
How Rx Detect Works

- Tx is required to detect when a Rx is added to the channel.
- Tx periodically sends out pulse looking for change in RC time constant
- which requires the Tx to have a receive circuit on the output.



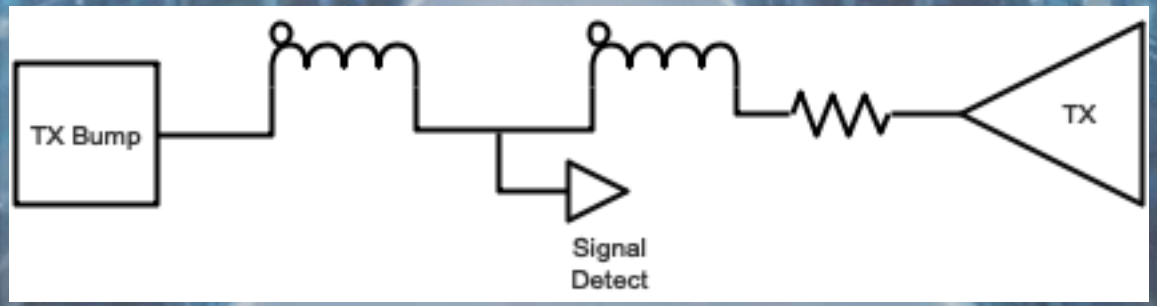
Blue is wave form when Rx has Rterm disabled
Red is wave form when Rx has Rterm enabled





Solution to challenge

- To enable the support of multiple standards the capacitance of these additional circuits need to be minimized.
- One technique that can be used to "hide" the extra load is to use on-die tcoil.
- A tcoil uses coupled inductors to increase the bandwidth and hide loading in the center tap of the coil.



Why make a multi standard SerDes

- For ASIC market having one IP to integrate that covers all needs:
  - Reduces Risk
  - Decreases time to market
  - Increases product flexibility
- For FPGA market having a multi standard SerDes is extremely important
  - One SerDes design to cover AI/ML, data center, telecommunications, high-performance computing and all other applications.

Summary

- SerDes enable large amounts of data to be communicated between to devices by serializing parallel data and running at higher data rates.
- When designing to accommodate a wide array of standards and data rates early planning is key.
- An example of how early planning and use of Tcoil can be used to enable required Rx detect circuits was shared
- Multi standard SerDes is key for FPGA markets to enable the widest ability of use in customer designs.